FIG_1

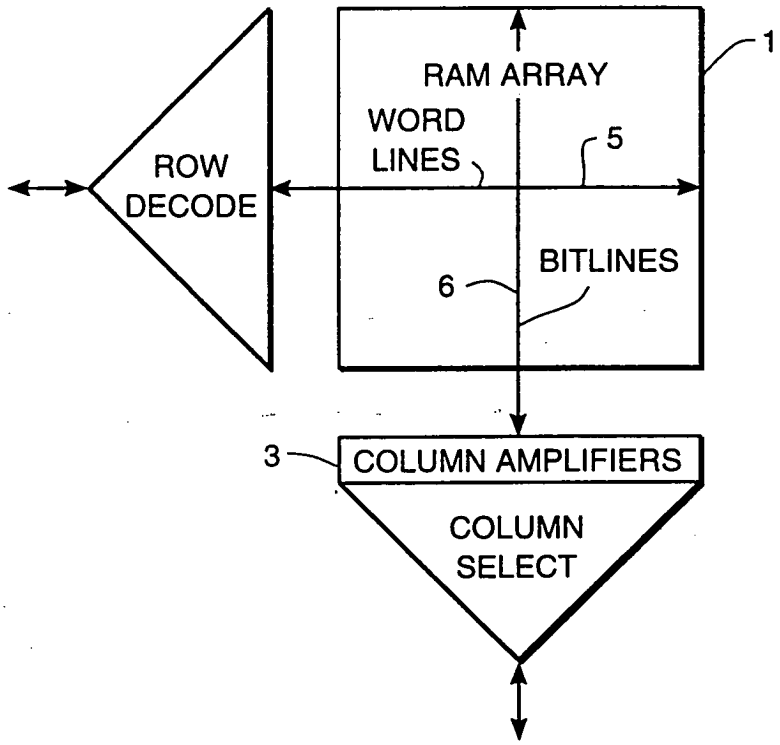


FIG_2

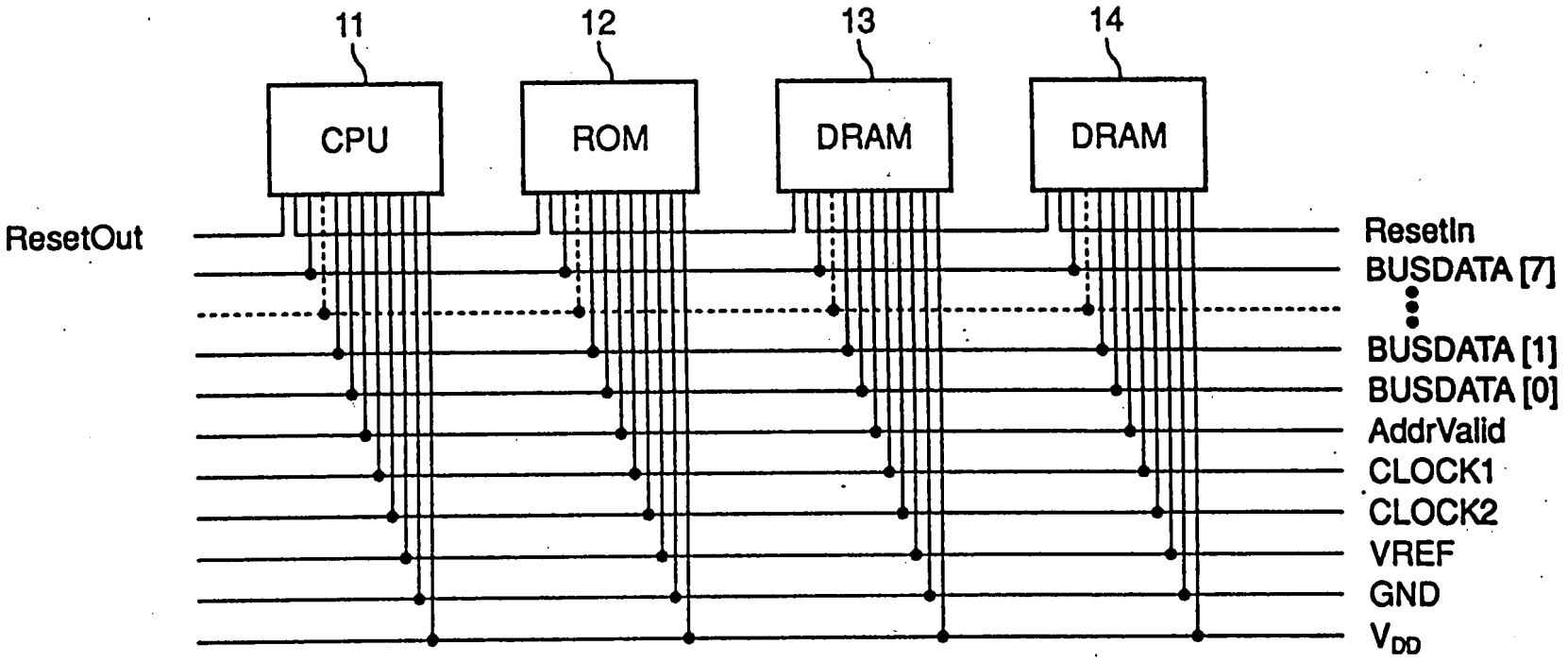
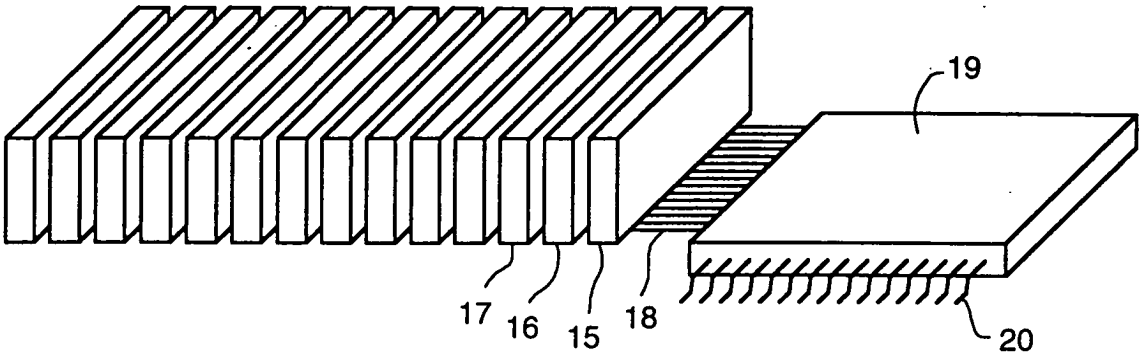


FIG_3



REGULAR ACCESS

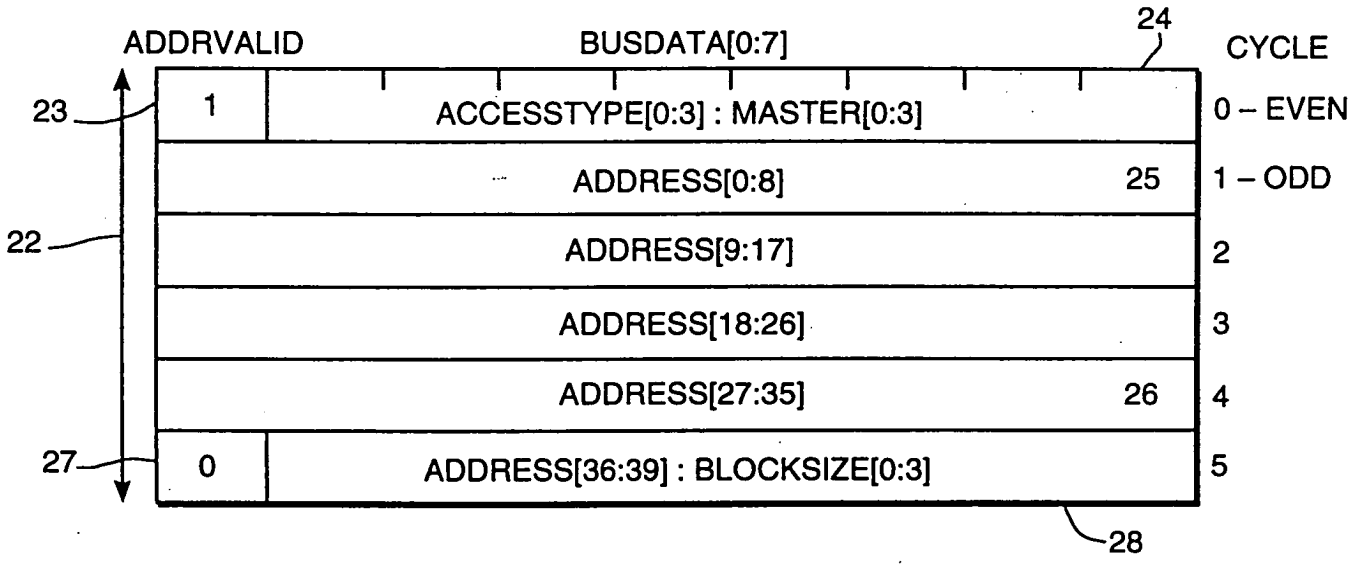


FIG_4

REJECT (NACK) CONTROL PACKET

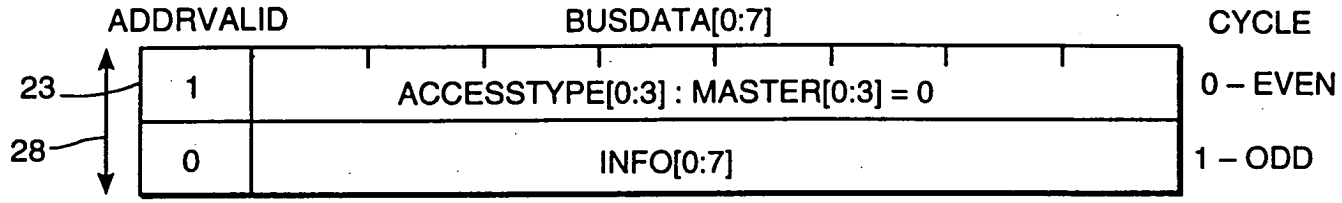


FIG_5

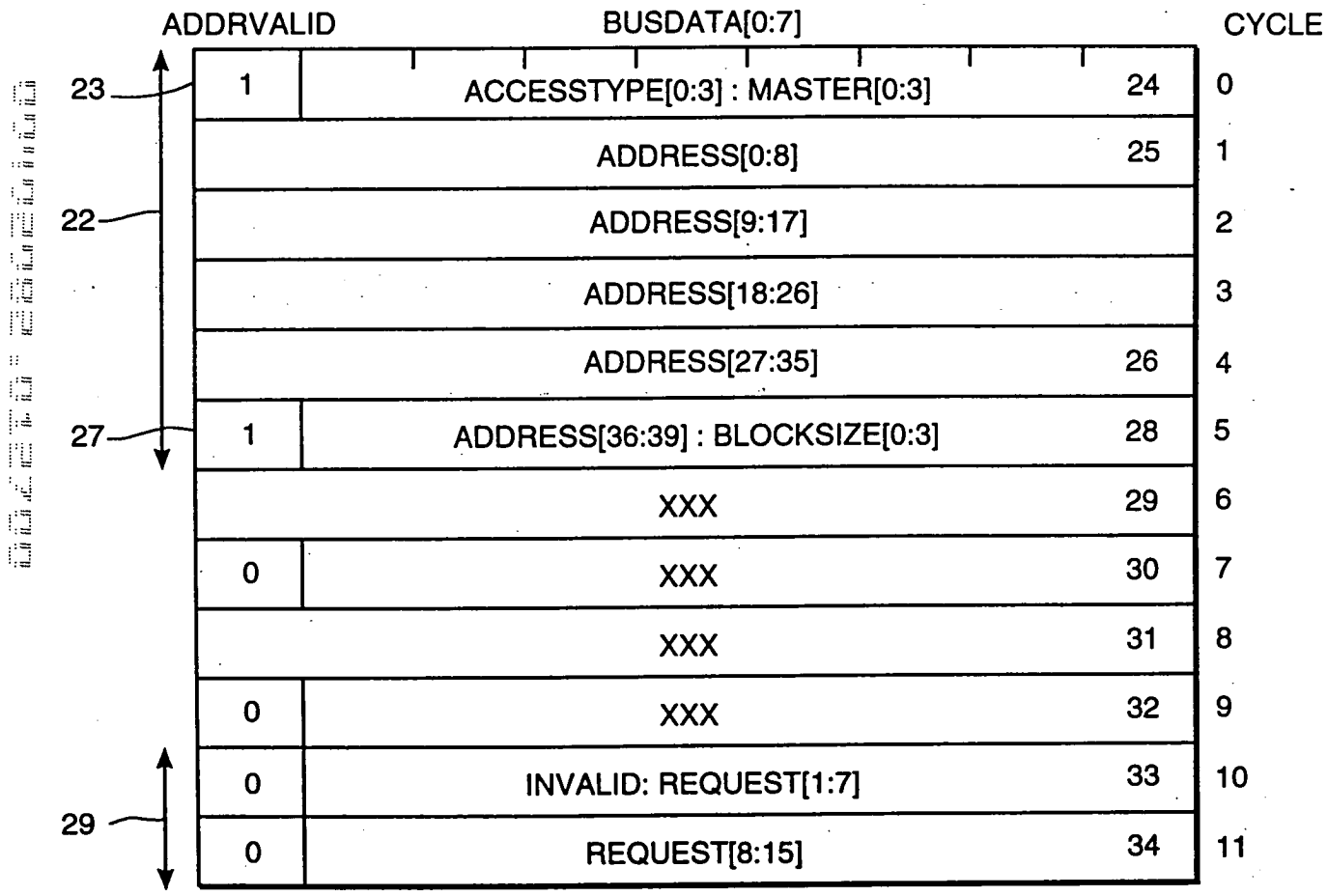


FIG_6

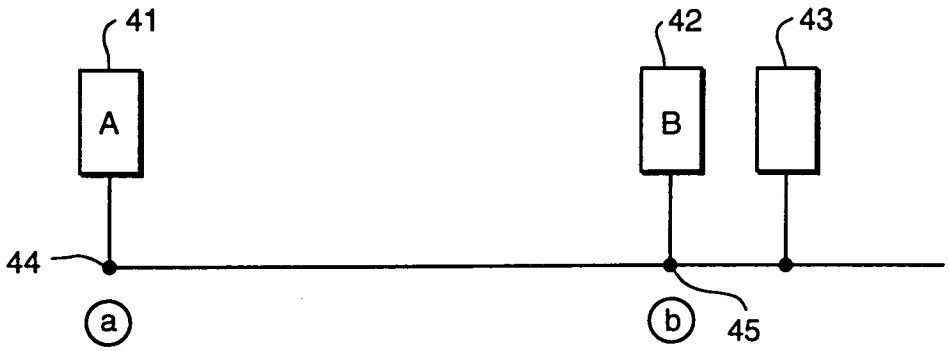


FIG_7A

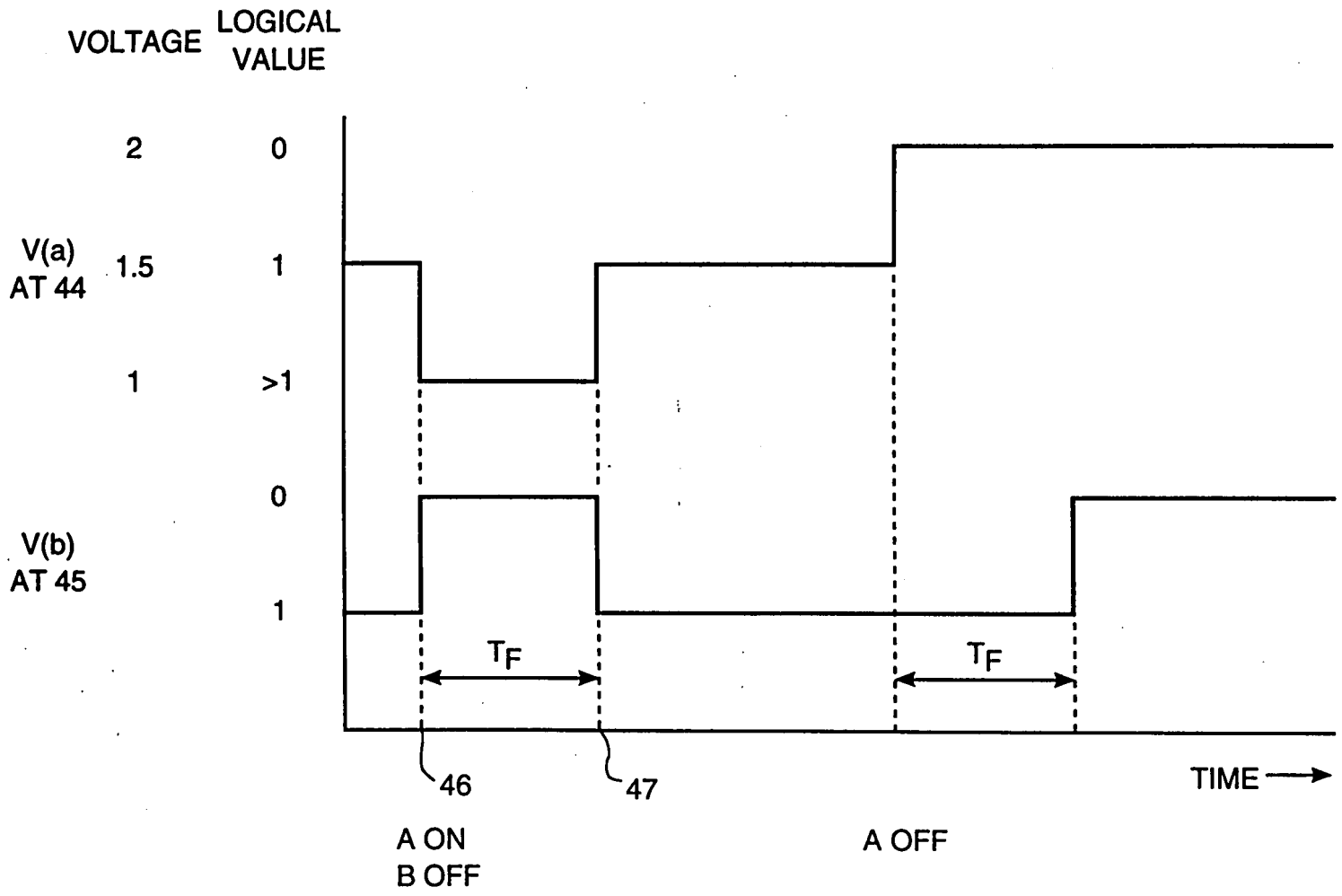


FIG_7B

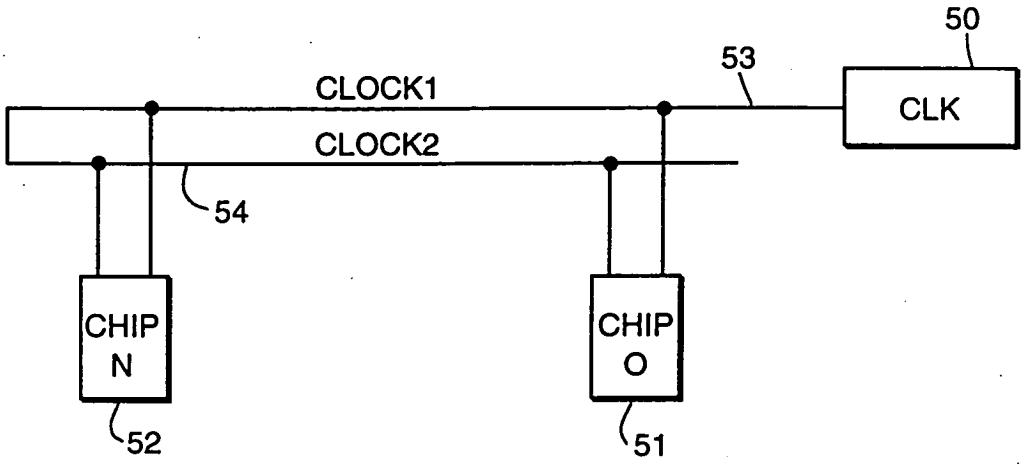

50
53
CLOCK1
CLK
CLOCK2
54
CHIP N
CHIP O
52
51

FIG_8A

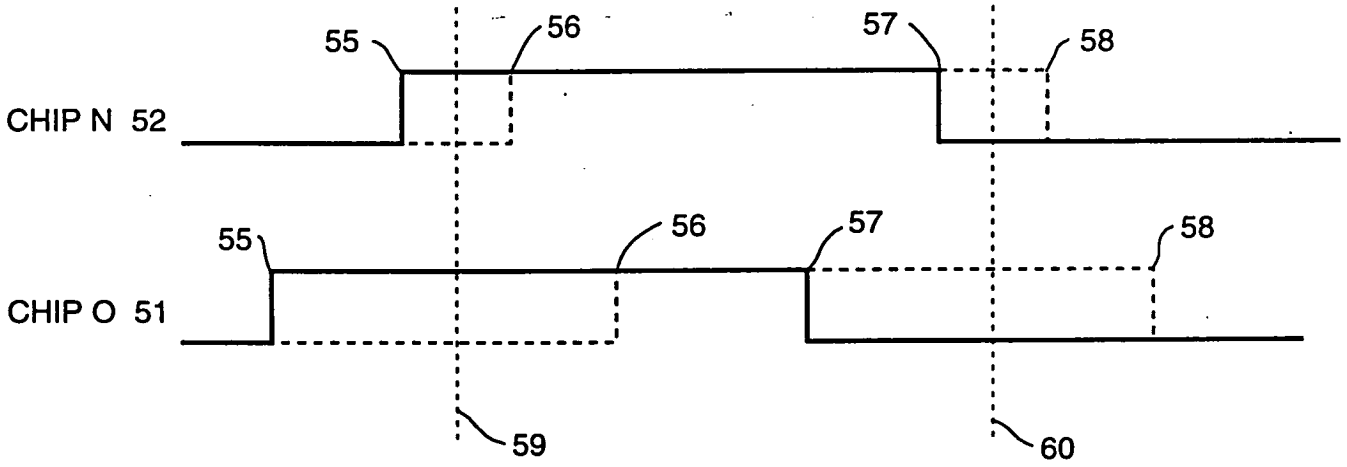
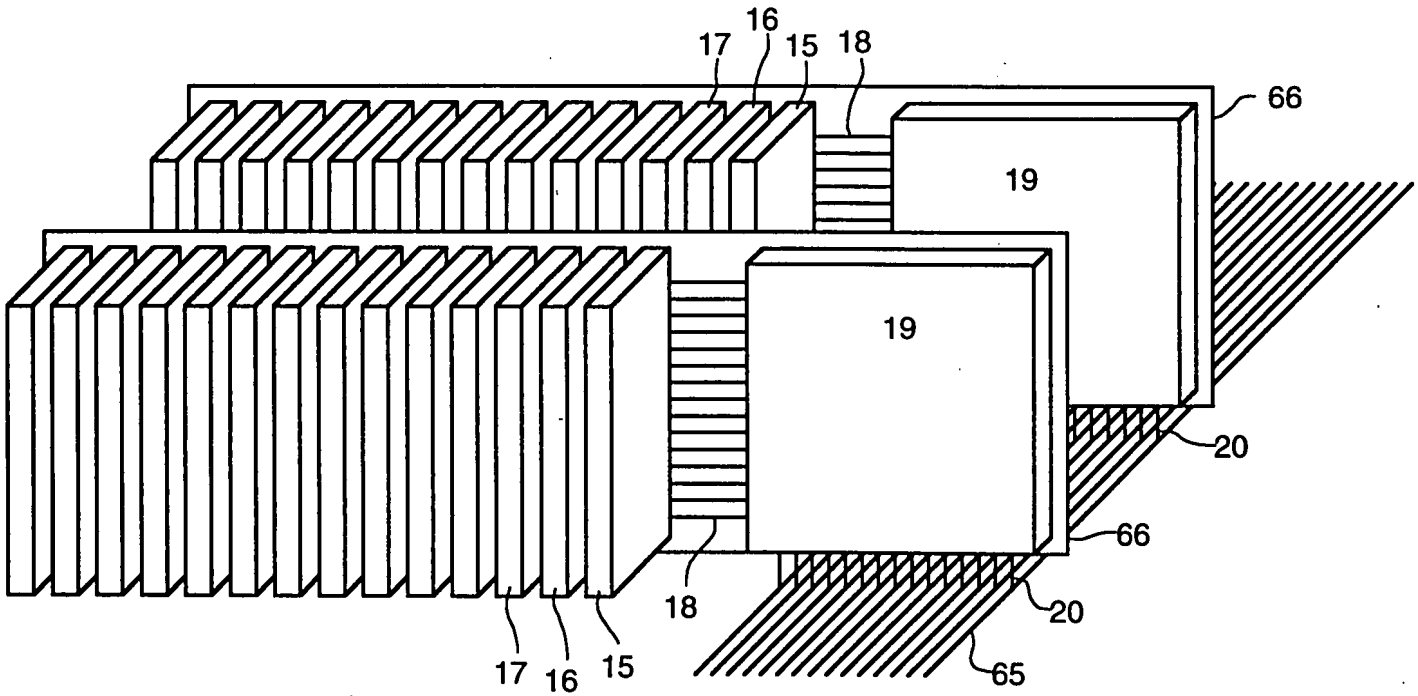

55
56
57
58
CHIP N 52
55
56
57
58
CHIP O 51
59
60

FIG_8B

FIG_9



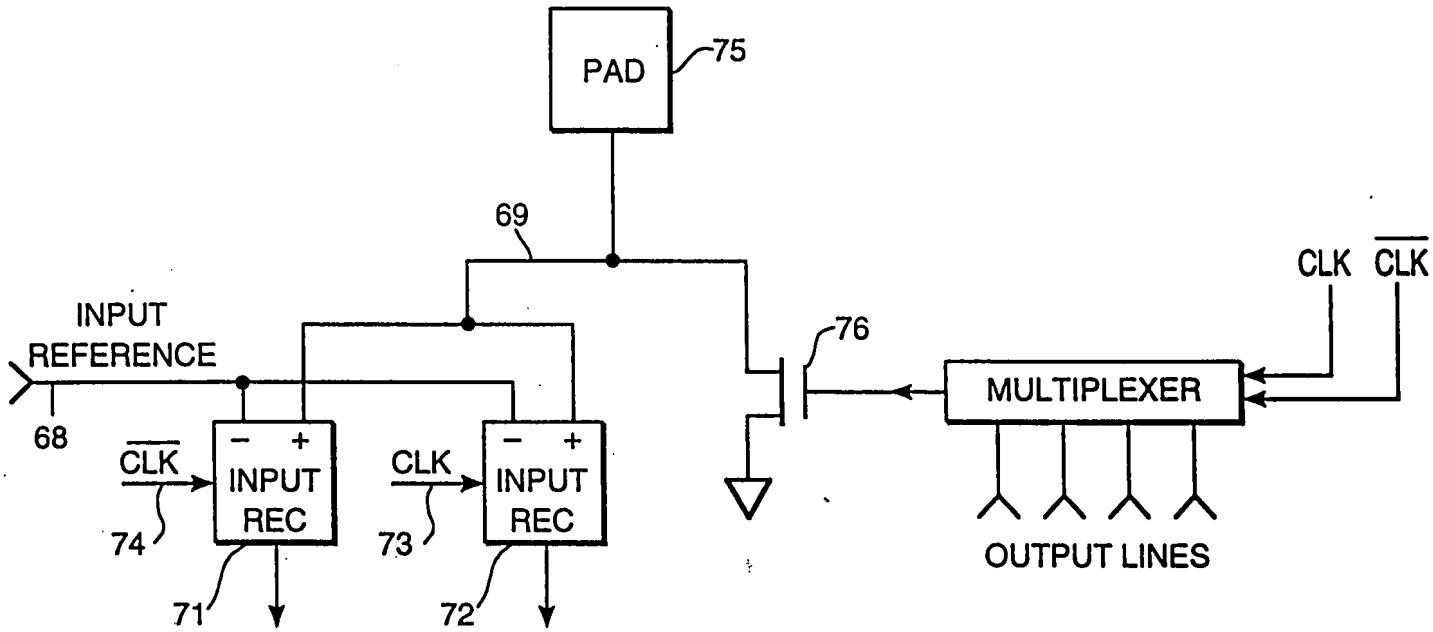

PAD
75
69
INPUT
REFERENCE
68
CLK
74
INPUT
REC
71
CLK
73
INPUT
REC
72
76
MULTIPLEXER
CLK
CLK
OUTPUT LINES

FIG_10

FIG_11

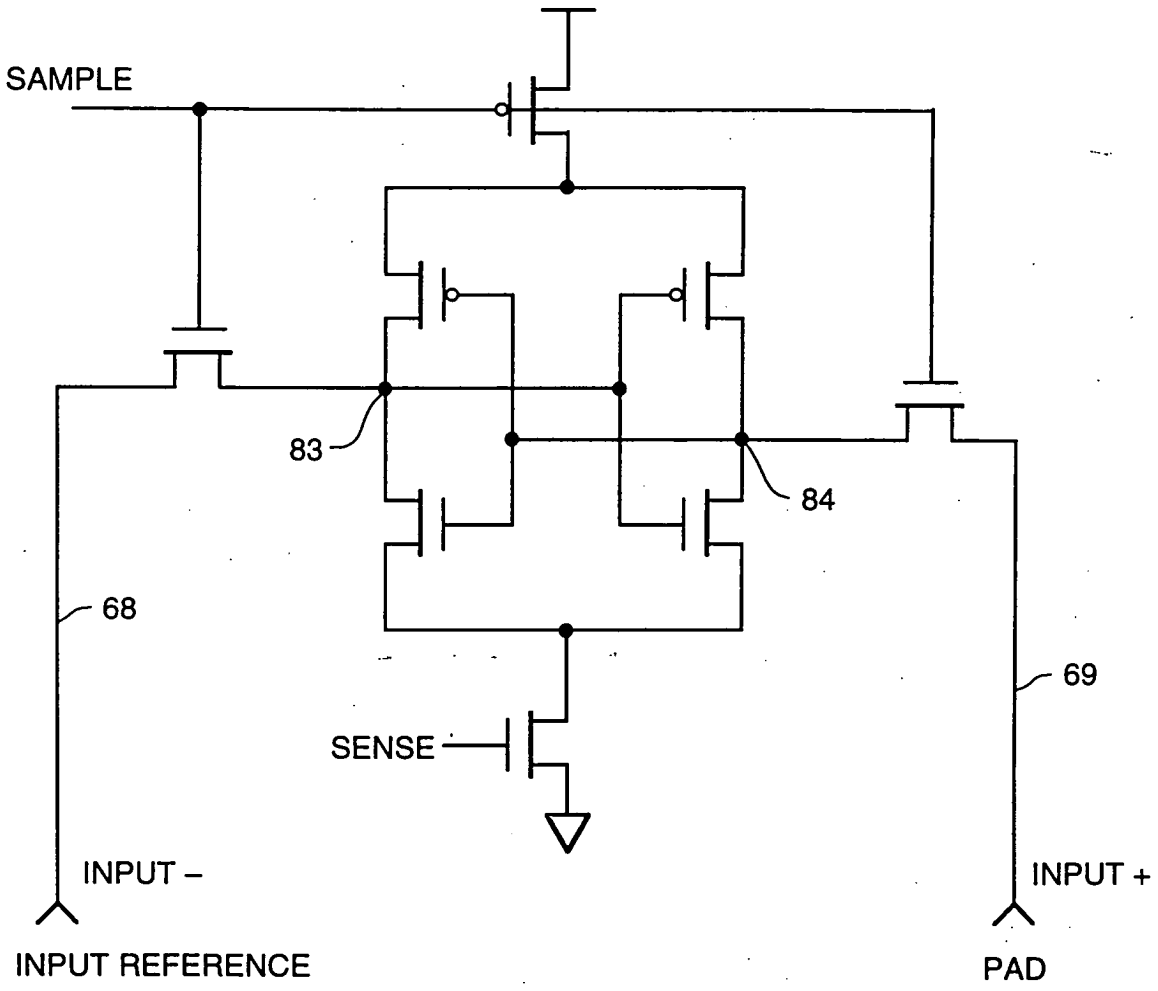


FIG_12

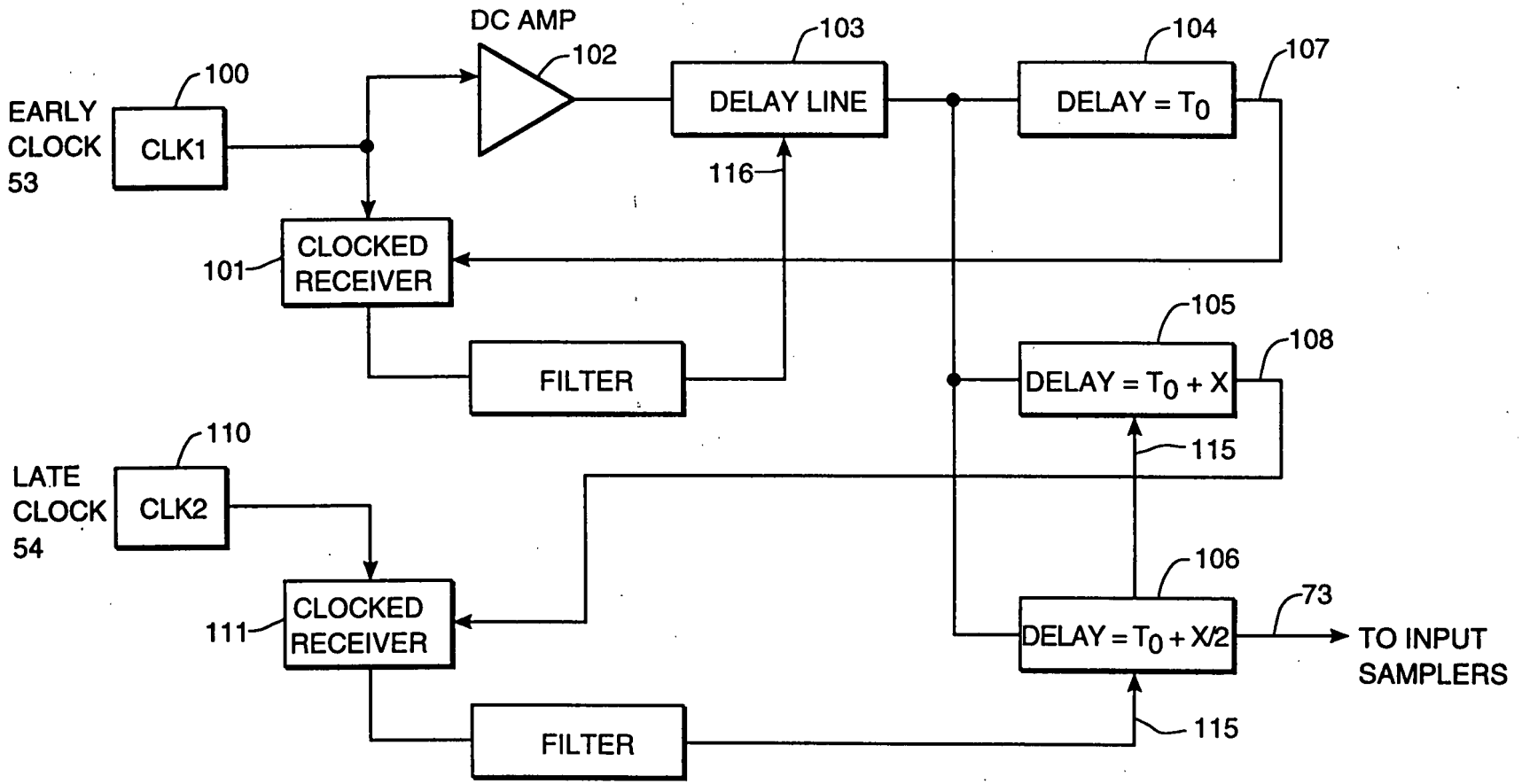
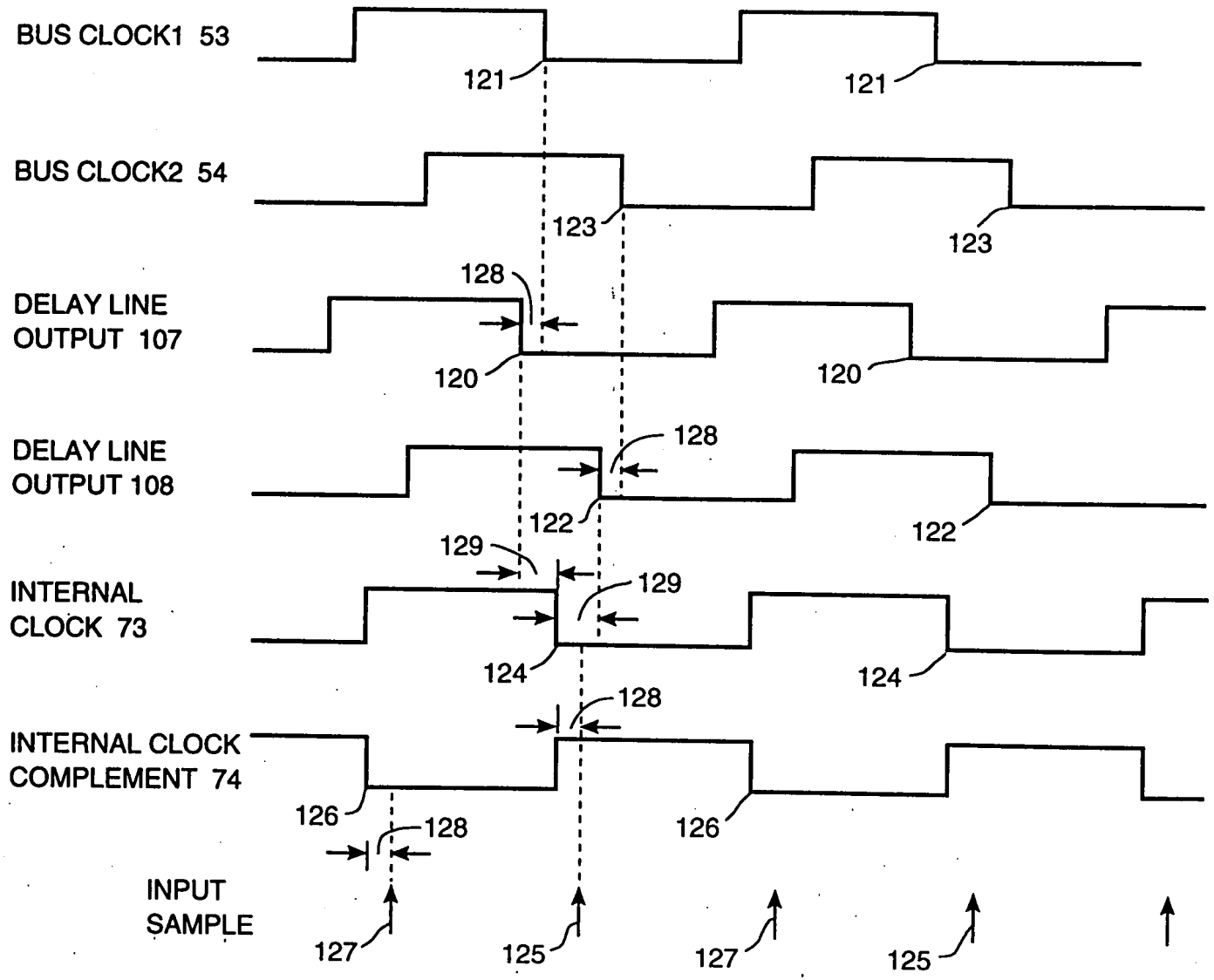


FIG_13



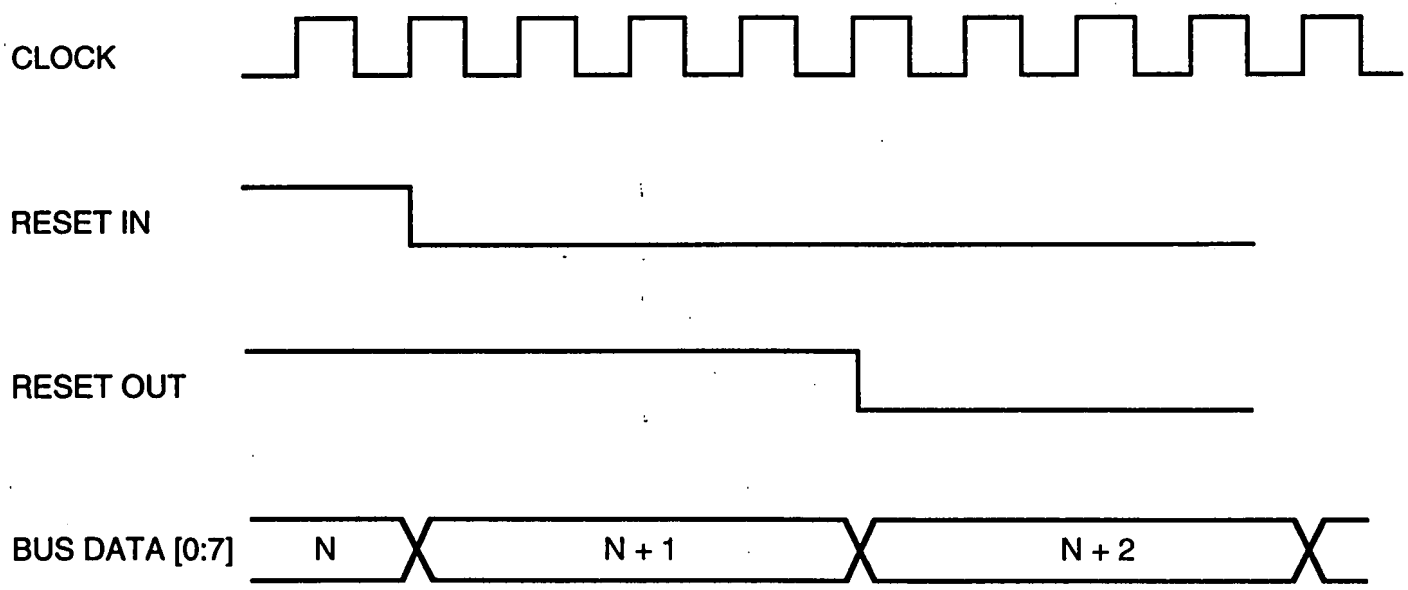
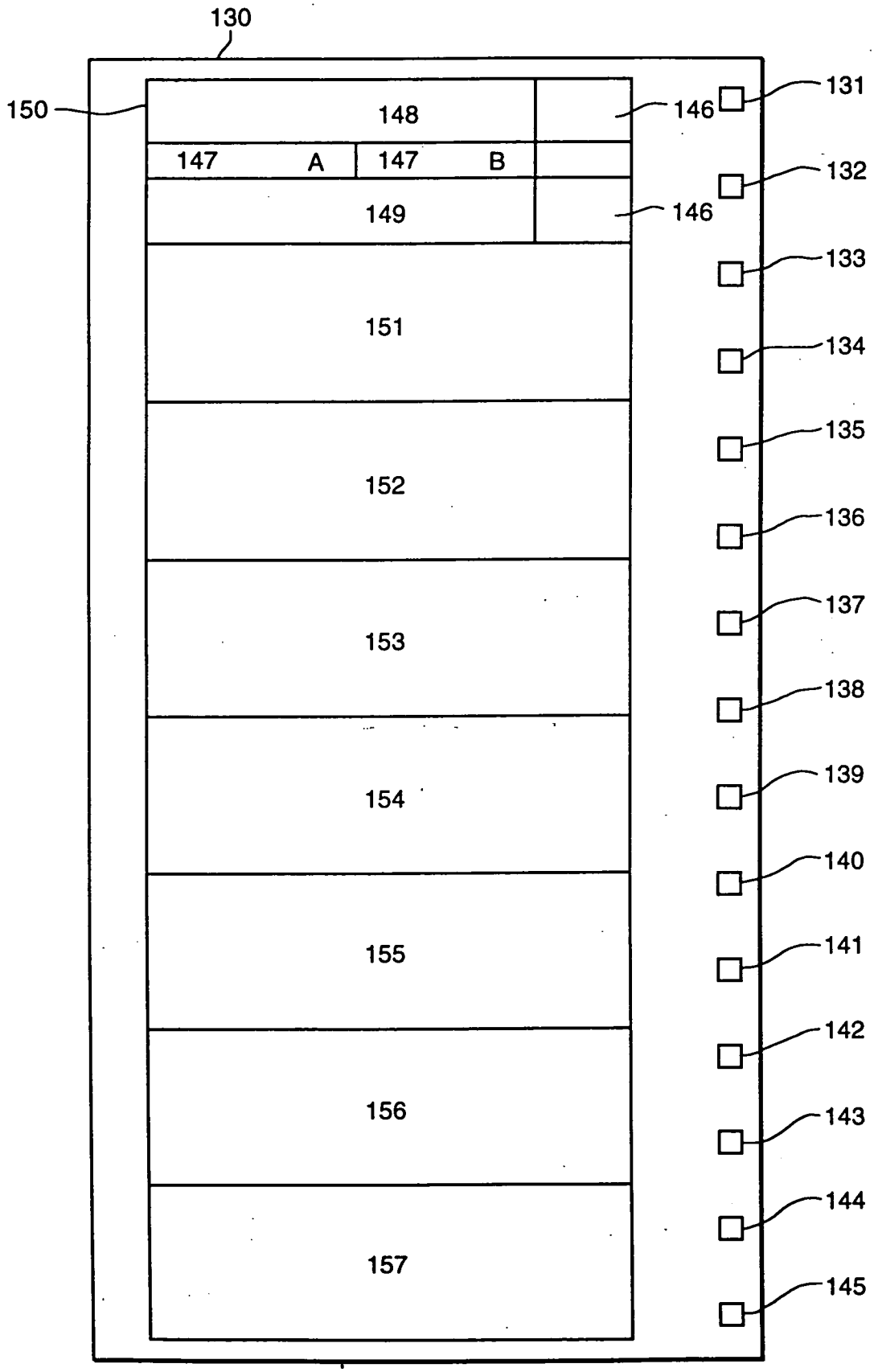


FIG_14

FIG_15


130
150
148
146
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A
147
B
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